REMARKS/ARGUMENTS

Applicant would like to thank the Examiner for the careful consideration given the present application. The application has been carefully reviewed in light of the Office action, and amended as necessary to more clearly and particularly describe the subject matter which applicant regards as the invention.

The Examiner has required corrected drawings in accordance with proposed drawing corrections already approved by the Examiner. Accordingly, corrected formal drawings are enclosed herewith.

The Examiner has required a substitute specification in proper idiomatic English. An appropriate substitute specification in compliance with 37 CFR § 1.52(a) and (b) is included herewith. The substitute specification contains no new matter.

Claims 1-4 were rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,117,377 to Finman (hereinafter "Finman") in view of "Pattern-Independent Current Estimation for Reliability Analysis of CMOS Circuits" by Burch et al. (hereinafter "Burch"). For the following reasons, the rejection is respectfully traversed.

The subject matter of Finman, relating to a electromagnetic *signal* analyzer which *measures* a signal from a test path, is not at all analogous to the subject matter of the invention, which pertains to a method of analyzing electromagnetic *interference* generated by a large scale integrated circuit (LSI) using a *mathematical simulation* of the LSI. See MPEP §2141.01(a). The similarities and differences in structure and function of the inventions carry great weight in determining if art is analogous. See In re Ellis, 476 F.2d 1370, 1372, 177 USPQ 526, 527 (CCPA 1973). The functions of the devices are quite different. The signal analyzer of Finman measures and analyzes characteristics of an actual electromagnetic signal received by the analyzer from a network to which it is physically connected. In contrast, the function of the invention is a different field of endeavor, providing a method for using a mathematical model of an LSI to analyze electromagnetic interference generated by the LSI. No actual

electromagnetic signals are analyzed or physical connections to a network are utilized. Accordingly, the reference is not reasonably pertinent to the problem with which the inventor is concerned because a person having ordinary skill in the art of electrical circuit simulation would not reasonably have expected to solve that problem by considering a reference dealing with an electromagnetic signal analyzer. See In re Clay, 966 F.2d 656, 23 USPQ2d 1058 (Fed. Cir. 1992). Thus, the rejection under 35 U.S.C. 103(a) based on Finman is not proper.

Further, one of ordinary skill in the art would not find a suggestion or motivation in the prior art to modify the teachings of the signal analyzer of Finman with the circuit simulation techniques disclosed in the Burch article, as required to form a *prima facie* case of obviousness. The Examiner is respectfully reminded that, "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be *found in the prior art, and not based on applicant's disclosure.*" (See MPEP § 2142 citing *In re Vaeck,* 20 USPQ2d 1438 (Fed. Cir. 1991).) The Examiner states that such a combination or modification "would have allowed the skilled artisan to determine the worst case current waveform." It is respectfully submitted that this is merely a statement of a benefit *from the presently claimed invention*, rather than a motivation or suggestion in the *prior art*. Thus, a *prima facie* showing of obviousness has not been sufficiently established for the purposes of 35 U.S.C. 103.

Claims 5-8 were rejected under 35 U.S.C. 103(a) over U.S. Patent No. 5,784,285 to Tamaki et al. (hereinafter "Tamaki") in view of Burch. For the following reasons, the rejection is respectfully traversed.

As with Finman as explained above, the subject matter of Tamaki, relating to a waveform analyzer which analyzes *measured* data collected from an actual electronic device by an electromagnetic detector, is not at all analogous to the simulation method which analyzes *theoretical* data calculated based on a mathematical model of an electronic device. Thus, the rejection under 35 U.S.C. 103(a) based on Tamaki is not proper.

Moreover, since the present invention performs superimposing of a clock signal, a noise characteristic of the clock cycle can be modeled. None of the cited references teaches or suggests superimposing a clock signal. Applicant respectfully submits that the cited art is not substantially related to the presently claimed invention.

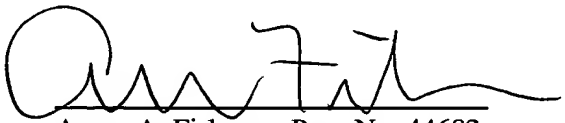
Further, as with the rejection based on Finman, one of ordinary skill in the art would not find a suggestion or motivation in the prior art to modify the teachings of the waveform analyzer of Tamaki with the circuit *simulation* techniques disclosed in the Burch article, as required to form a *prima facie* case of obviousness. The Examiner states the same reason for the combination as with the combination of Finman and Burch. Thus, for substantially the same reasons as discussed above, a *prima facie* showing of obviousness has not been sufficiently established for the purposes of 35 U.S.C. 103.

In light of the foregoing, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the Examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No. 32809.

Respectfully submitted,

PEARNE & GORDON LLP

By: 
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